

General Description

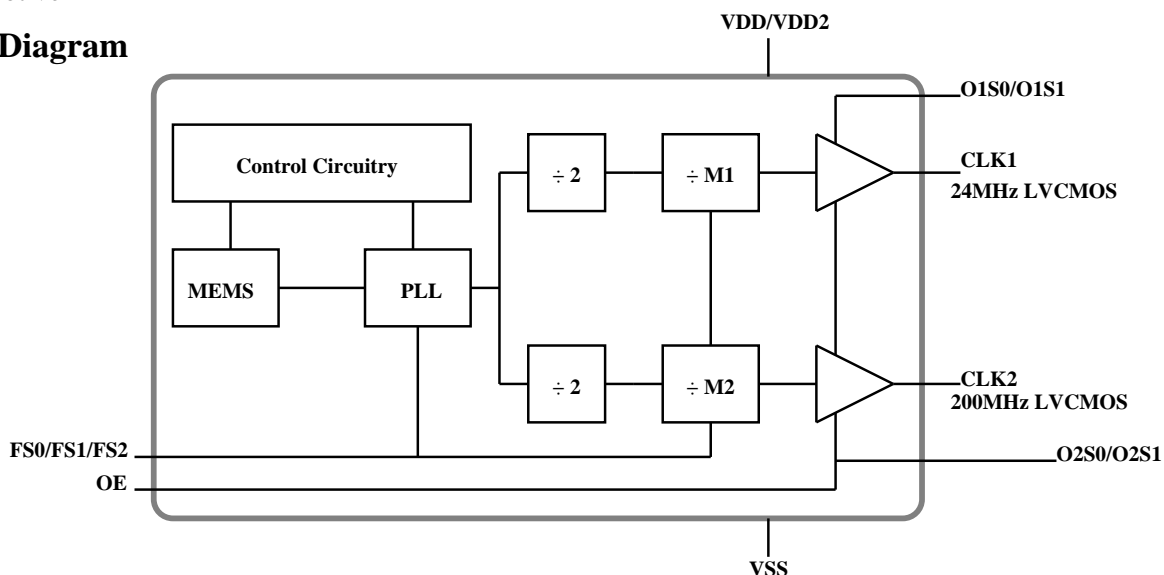
The DSC2011FI2-F0017 is a programmable, high performance dual LVC MOS output oscillator utilizing Micrel's proven silicon MEMS technology to provide excellent jitter and stability while incorporating additional device functionality. Two LVC MOS outputs are controlled by separate supply voltages to allow for independent voltage level control. The frequencies of the outputs can be identical or independently derived from a common PLL frequency source.

The DSC2011FI2-F0017 has provision for up to eight user-defined pre-programmed, pin-selectable output frequency combinations. The DSC2011FI2-F0017 is also equipped with independent pin-selectable output drive strengths to reduce EMI and noise.

Applications

- Consumer Electronics
- Storage Area Networks
 - SATA, SAS, Fibre Channel
- Passive Optical Networks
 - EPON, 10G-EPON, GPON, 10G-GPON
- Ethernet
 - 1G, 10GBASE-T/KR/LR/SR, and FCoE
- HD/SD/SDI Video & Surveillance
- PCI Express
- Automotive

Block Diagram



Features

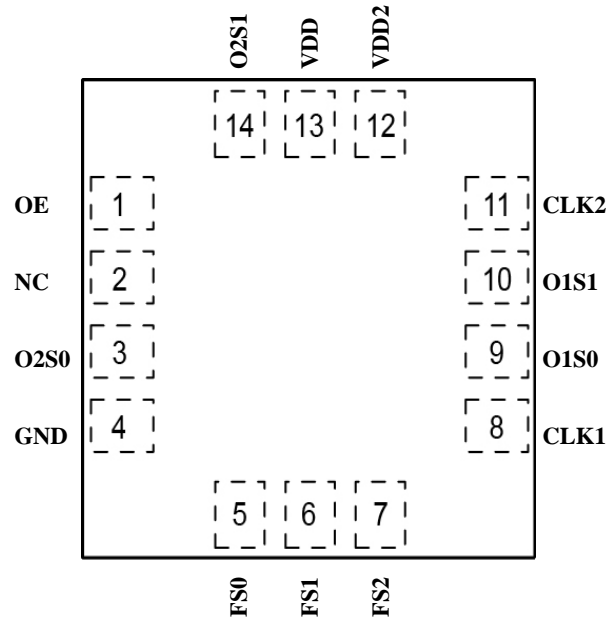
- Frequency and output formats:
 - LVC MOS 24/24MHz
 - LVC MOS 200/100MHz
- Low RMS phase jitter: <1ps (typ)
- ±25ppm frequency stability
- -40°C to +85°C industrial temperature range
- High supply noise rejection: -50dBc
- Pin-selectable configurations
 - 2-bit output drive strength
 - Up to 8 output frequency combinations
- Separate power supply (VDD2) for CLK2
- Excellent shock & vibration immunity
 - Qualified to MIL-STD-883
- High reliability
 - 20x better MTF than quartz oscillators
- Supply range of 2.25 to 3.6V
- AEC-Q100 automotive qualified
- 14-pin 3.2mm x 2.5mm QFN package

Ordering Information

| Ordering Part Number | Industrial Temperature Range | Shipping | Package |
|----------------------|------------------------------|---------------|--------------------------|
| DSC2011FI2-F0017 | -40°C to +85°C | Tube | 14-pin 3.2mm x 2.5mm QFN |
| DSC2011FI2-F0017T | -40°C to +85°C | Tape and Reel | 14-pin 3.2mm x 2.5mm QFN |

Devices are Green and RoHS compliant. Sample material may have only a partial top mark.

Pin Configuration



14-pin 3.2mm x 2.5mm QFN

Pin Description

| Pin Number | Pin Name | Pin Type | Pin Function |
|------------|----------|----------|--|
| 1 | OE | I | Enables outputs when high and disables outputs when low |
| 2 | NC | | Leave unconnected or connect to ground |
| 3 | O2S0 | I | Least significant bit for drive strength selection for CLK2, see Table 1 for details |
| 4 | GND | PWR | Ground |
| 5 | FS0 | I | Least significant bit for frequency selection, see Table 2 for details |
| 6 | FS1 | I | Middle bit for frequency selection, see Table 2 for details |
| 7 | FS2 | I | Most significant bit for frequency selection, see Table 2 for details |
| 8 | CLK1 | O | LVC MOS output |
| 9 | O1S0 | I | Least significant bit for drive strength selection for CLK1, see Table 1 for details |
| 10 | O1S1 | I | Most significant bit for drive strength selection for CLK1, see Table 1 for details |
| 11 | CLK2 | O | LVC MOS output |
| 12 | VDD2 | PWR | Power supply for LVC MOS output CLK2, 1.65V to 3.6V ($VDD2 \leq VDD$) |
| 13 | VDD | PWR | Power supply |
| 14 | O2S1 | I | Most significant bit for drive strength selection for CLK2, see Table 1 for details |

Operational Description

The DSC2011FI2-F0017 is a dual output LVCMOS oscillator consisting of a MEMS resonator and a supporting PLL IC. The two LVCMOS outputs are generated through independent 8-bit programmable dividers from the output of the internal PLL. The two constraints are imposed on the output frequencies:

1) $f_2 = M \times f_1 / N$, where M and N are even integers between 4 and 254, 2) $1.2\text{GHz} < N \times f_2 < 1.7\text{GHz}$.

The actual frequencies output by DSC2011FI2-F0017 are controlled by an internal pre-programmed memory (OTP). This memory stores all coefficients required by the PLL for up to eight different frequency combinations. Three control pins (FS0 - FS2) select the output frequency combination.

DSC2011FI2-F0017 has independent control of the output voltage levels of the two outputs. The high voltage level of

CLK1 is equal to the main supply voltage, VDD (pin 13). VDD2 (pin 12) sets the high voltage level of CLK2. VDD2 must be equal to or less than VDD at all times to insure proper operation. VDD2 can be as low as 1.65V.

When OE (pin 1) is floated or connected to VDD, the DSC2011FI2-F0017 is in operational mode. Driving Enable to ground will tri-state both output drivers (hi-impedance mode).

DSC2011FI2-F0017 has programmable output drive strength for each output. Using two control pins (OXS0-OXS1) for each output, the drive strength can be independently adjusted to match circuit board impedances to reduce spower supply noise, overshoot/undershoot and EMI. Table 1 displays typical rise / fall times for the output with a 15pF load capacitance as a function of these control pins at VDD = 3.3V and room temperature.

| | Output Drive Strength Bits [OXS1, OXS0] - Default is [11] | | | |
|---------|---|-----|-----|------------|
| | 00 | 01 | 10 | 11 |
| tr (ns) | 1.6 | 1.4 | 1.2 | 1.1 |
| tf (ns) | 2.4 | 2.2 | 1.5 | 1.4 |

Table 1. Rise/Fall Times for Drive Strengths

Output Clock Frequencies

Frequency select bits are weakly tied high so if left unconnected the default setting will be [111] and the device will output the associated frequency highlighted in bold.

| Freq (MHz) | Freq Select Bits [FS2, FS1, FS0] - Default is [111] | | | | | | | |
|------------|---|-----|-----|-----|-----|-----|-----|------------|
| | 000 | 001 | 010 | 011 | 100 | 101 | 110 | 111 |
| CLK1 | 24 | NA | NA | NA | NA | NA | NA | 24 |
| CLK2 | 100 | NA | NA | NA | NA | NA | NA | 200 |

Table 2. Pin-Selectable Output Frequencies

Absolute Maximum Ratings

| Item | Min. | Max. | Units | Condition |
|----------------|------|-----------|-------|------------|
| Supply Voltage | -0.3 | +4.0 | V | |
| Input Voltage | -0.3 | VDD + 0.3 | V | |
| Junction Temp | - | +150 | °C | |
| Storage Temp | -55 | +150 | °C | |
| Soldering Temp | - | +260 | °C | 40sec max. |
| ESD | | | | |
| HBM | - | 4000 | V | |
| MM | - | 400 | | |
| CDM | - | 1500 | | |

1000+ years of data retention on internal memory

Specifications (Unless specified otherwise: T = 25°C, max LVC MOS drive strength)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Units |
|---|--------------|---|-----------------|--------------------|-----------------|-------|
| Supply Voltage ¹ | VDD VDD2 | VDD2 ≤ VDD | 2.25 1.65 | | 3.6 3.6 | V |
| Supply Current | IDD | OE pin low - outputs are disabled | | 21 | 23 | mA |
| Supply Current ² | IDD | OE pin high - outputs are enabled CL = 15pF, F01 = F02 = 125MHz | | 32 | | mA |
| Frequency Stability | ΔF | Includes frequency variation due to initial tolerance, temp. and power supply voltage | | | ±25 | ppm |
| Aging | ΔF | First year (@ 25°C) | | | ±5 | ppm |
| Startup Time ³ | tSU | T = 25°C | | | 5 | ms |
| Input Logic Levels Input Logic High Input Logic Low | VIH VIL | | 0.75 x VDD - | | - 0.25 x VDD | V |
| Output Disable Time ⁴ | tDA | | | | 5 | ns |
| Output Enable Time | tEN | | | | 20 | ns |
| Pull-Up Resistor ² | | Pull-up exists on all digital IO | | 40 | | kOhms |
| LVC MOS Outputs | | | | | | |
| Output Logic Levels Output Logic High Output Logic Low | VOH VOL | I = ±6mA | 0.9 x VDD - | | - 0.1 x VDD | V |
| Output Transition Time ⁴ Rise Time Fall Time | tR tF | 20% to 80% CL = 15pF | | 1.1 1.4 | 2 2 | ns |
| Frequency | CLK1 CLK2 | [FS2, FS1, FS0] = [1, 1, 1] | | 24 200 | | MHz |
| Output Duty Cycle | SYM | | 45 | | 55 | % |
| Period Jitter ⁵ | JPER | F01 = F02 = 125MHz | | 3 | | psRMS |
| Integrated Phase Noise | JPH | 200kHz to 20MHz @ 125MHz 100kHz to 20MHz @ 125MHz 12kHz to 20MHz @ 125MHz | | 0.3 0.38 1.7 | 2 | psRMS |

Notes:

- Pin 12 VDD2, and pin 13 VDD should be filtered with 0.1uF capacitors.
- Output is enabled if OE pin is floated or not connected.
- tSU is time to 100ppm stable output frequency after VDD is applied and outputs are enabled.
- Output Waveform and Test Circuit figures below define the parameters.
- Period Jitter includes crosstalk from adjacent output.

Nominal Performance Parameters (Unless specified otherwise: T = 25°C, VDD = 3.3V)



Figure 1. LVC MOS Phase Jitter (integrated phase noise)

LVC MOS Output Waveform



Figure 2. LVC MOS Output Waveform

| MSL 1 @ 260°C refer to JSTD-020C | |
|-----------------------------------|--------------|
| Ramp-Up Rate (200°C to Peak Temp) | 3°C/sec Max. |
| Preheat Time 150°C to 200°C | 60 - 180 sec |
| Time maintained above 217°C | 60 - 150 sec |
| Peak Temperature | 255 - 260°C |
| Time within 5°C of actual Peak | 20 - 40 sec |
| Ramp-Down Rate | 6°C/sec Max. |
| Time 25°C to Peak Temperature | 8 min Max. |

Solder Reflow Profile

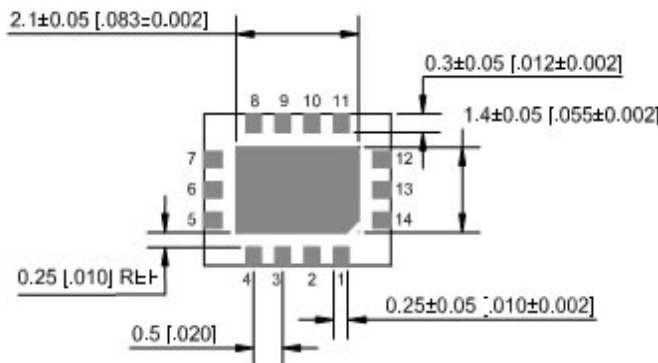
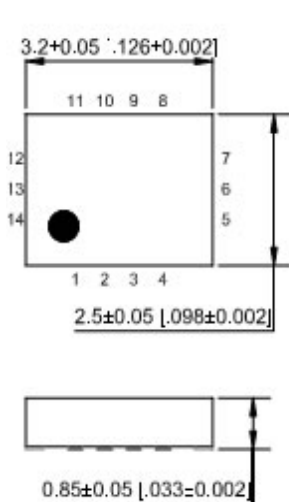


Figure 3. Solder Reflow Profile

Package Information⁷

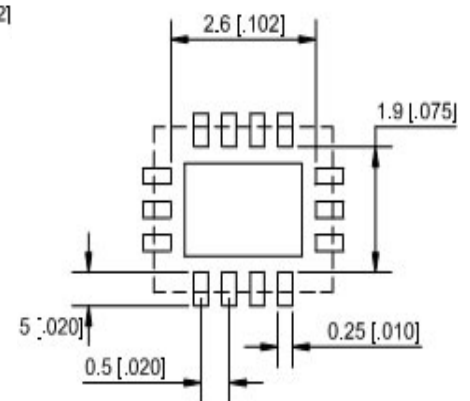
External Dimensions

units: mm[inch]



Recommended Solder Pad Layout

units: mm[inch]



3.2mm x 2.5mm 14 Lead Plastic Package

Notes:

- 6. Connect the exposed die paddle to ground.
- 7. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

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