

## Description

The ISL54220IRUEVAL1Z evaluation board is designed to provide a quick and easy method for evaluating the ISL54220 USB Switch IC.

The ISL54220 device is a unique IC. To use this evaluation board properly requires a thorough knowledge of the operation of the IC. Refer to the data sheet for an understanding of the functions and features of the device. Studying the device's truth-table along with its pinout diagram is the best way to get a quick understanding of how the part works.

A picture of the main evaluation board is shown in Figure 1. The ISL54220  $\mu$ TQFN IC is soldered onto the evaluation board. It is located in the center of the board and is designated as U1.

The evaluation board contains USB connectors to allow the user to easily interface with the IC to evaluate its functions, features, and performance. For example, with the board properly powered and configured, as shown in Figure 2, you can control the logic pins, SE and  $\overline{OE}$ , to switch between the two high-speed USB devices while connected to a single USB host (computer).

In a typical application, the ISL54220 dual SPDT device is used to select between two different USB transceiver sections of a media player. Logic control from a  $\mu$ processor determines which section to connect to the computer. To change channels, the following sequence would possibly be followed:

1. A signal would be sent to take the  $\overline{OE}$  pin High, to open all switches. The off-isolation of the ISL54220 device would allow the present active channel to properly disconnect from the computer.
2. The SEL pin would be set to select the other USB channel.
3. The  $\overline{OE}$  pin would then be taken Low to close the switches to make the connection between the computer and the other USB section of the player.

This application note will guide the user through the process of configuring and using the evaluation board to evaluate the ISL54220 device.

## Features

- Standard USB Connectors
- Standard Banana Jacks for Power, Ground,  $V_{BUS}$  and Logic Connections
- Jumpers to Allow a Device to be Powered through the Host Controller
- Convenient Test Points and Connections for Test Equipment

## Picture of Evaluation Board (Top View)

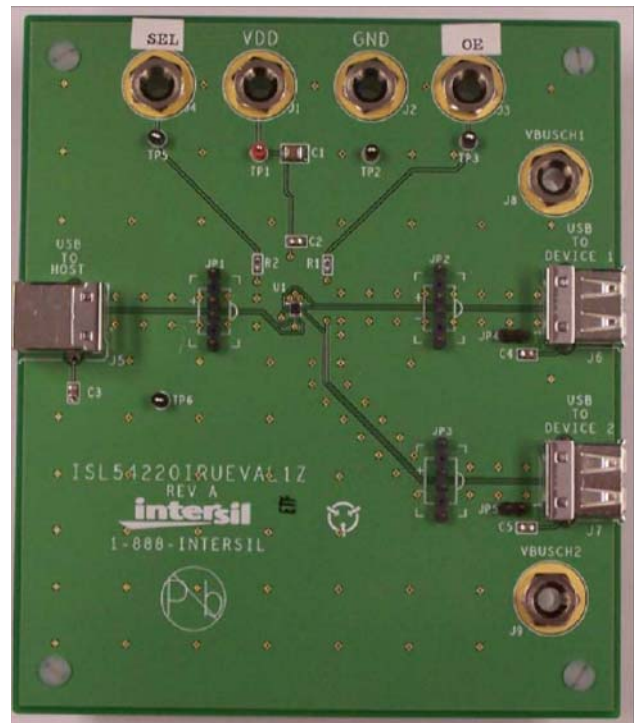


FIGURE 1. ISL54220IRUEVAL1Z EVALUATION BOARD

## Board Architecture/Layout

### Basic Layout of Evaluation Board

The basic layout of the main board is as follows: Refer to Figure 1.

- Power and Ground connections are at the top of the board at banana jacks (J1 and J2).
- Logic connections, SEL and  $\overline{OE}$ , are at the top of the board at banana jacks (J4 and J3).
- USB connection to an upstream host controller (Computer) is made at J5, located on the left side of the board.
- USB connections to downstream USB devices are made at connectors J6 and J7, located on right side of the board.
- $V_{BUS}$  voltage for the USB devices are made through banana jacks J8 and J9. Optionally,  $V_{BUS}$  for the USB devices can be connected to the Host Controller  $V_{BUS}$  through jumpers JP4 and JP5.
- Located in the center of the board is the ISL54220 IC (U1). The evaluation board has a pin 1 dot, to show how the IC should be oriented on to the evaluation board. The IC pin 1 indicator dot needs to be aligned with the evaluation board pin 1 dot indicator.

### IC Power Supply

A DC power supply connected at banana jacks J1 (VDD) and J2 (GND) provides power to the ISL54220 IC. The IC requires a 2.7VDC to 5.5VDC power supply for proper operation. The power supply should be capable of delivering 100 $\mu$ A of current.

### $V_{BUS}$ Power Supply

A DC power supply connected at banana jacks J8 (VBUSCH1) and J9 (VBUSCH2) provides the  $V_{BUS}$  voltage required by the USB devices. The devices require a DC power supply in the range of 4.4V to 5.25V for proper operation. The power supply should be capable of delivering 100 $\mu$ A of current.

The J8 banana jack is connected to the  $V_{BUS}$  pin of the J6 "A" type USB receptacle. The J9 banana jack is connected to the  $V_{BUS}$  pin of the J7 "A" type receptacle.

The  $V_{BUS}$  voltage can be provided from the USB host controller (computer) by installing a jumper at either JP4 or JP5.

With a jumper at JP4, the  $V_{BUS}$  voltage from J5 gets routed to the J6 connector. With this jumper installed, no DC supply should be connected at the J8 (VBUSCH1) banana jack.

With a jumper at JP5, the  $V_{BUS}$  voltage from J5 gets routed to the J7 connector. With this jumper installed, no DC supply should be connected at the J9 (VBUSCH2) banana jack.

### Logic Control

The state of the ISL54220 device is determined by the voltage at the SEL pin and the  $\overline{OE}$  pin. Access to the SEL pin is through the banana jack J4 (SEL) and access to the  $\overline{OE}$  pin is through the banana jack J3 ( $\overline{OE}$ ).

If SEL is driven Low (to ground) and EN = Low (to ground), the high-speed (HS) Channel 1 switches will be ON. In this state, the USB host controller (computer) connected at J5 will be connected through to the USB device connected at J6 and data will be able to be transmitted between the computer and the device.

If SEL is driven High (>1.4V) and EN = Low (to ground), the high-speed (HS) Channel 2 switches will be ON. In this state, the USB host controller (computer) connected at J5 will be connected through to the USB device connected at J7 and data will be able to be transmitted between the computer and the device.

If  $\overline{OE}$  = High (>1.4V), all switches will be OFF. Neither device will be connected through to the host controller.

In a typical application, the ISL54220 dual SPDT device is used to select between two different USB transceiver sections of a media player. Logic control from a  $\mu$ processor determines which section to connect to the computer. To change channels, the following sequence would possibly be followed:

1. A signal would be sent to take the  $\overline{OE}$  pin High, to open all switches. The off-isolation of the ISL54220 device would allow the present active channel to properly disconnect from the computer.
2. Then the SEL pin would be set to select the other USB channel.
3. The  $\overline{OE}$  pin would then be taken Low to close the switches to make the connection between the computer and the other USB section of the player.

### USB Connections

A "B" type USB receptacle labeled "USB TO HOST" (J5) is located on the left side of the board. This receptacle should be connected, using a standard USB cable, to the upstream USB host controller, which is usually a PC computer or hub. When this connection is made, the ISL54220 device will connect the computer through to the USB device determined by the voltage at the SEL logic control pin.

An "A" type USB receptacle labeled "USB TO DEVICE 1" (J6) is located on the right side of the board. The USB device can be plugged directly into this receptacle or through a standard USB cable.

An "A" type USB receptacle labeled "USB TO DEVICE 2" (J7) is located on the right side of the board. The USB device can be plugged directly into this receptacle or through a standard USB cable.

The USB switches are bi-directional, which allows the host (computer) and downstream USB device to both send and receive data.

### High-Speed Switches

The four HSx switches (HSD1-, HSD1+, HSD2-, HSD2+) are bi-directional switches that can pass rail-to-rail signals. When powered with a 3.3V supply, these switches have a nominal  $r_{ON}$  of  $6\Omega$  over the signal range of 0V to 400mV with a  $r_{ON}$  flatness of  $0.94\Omega$ . The  $r_{ON}$  matching between the HSDx- and HSDx+ switches over this signal range is only  $0.117\Omega$  ensuring minimal impact by the switches to USB high speed signal transitions. As the signal level increases, the  $r_{ON}$  switch resistance increases. At signal level of 3.3V the switch resistance is nominally  $129\Omega$ .

The HSx switches were specifically designed to pass USB 2.0 high-speed (480Mbps) differential signals typically in the range of 0V to 400mV. They have low capacitance and high bandwidth to pass the USB high-speed signals with minimum edge and phase distortion to meet USB 2.0 high speed signal quality specifications.

The HSx switches can also pass USB full-speed signals (12Mbps) with minimal distortion and meet all the USB requirements for USB 2.0 full-speed signaling.

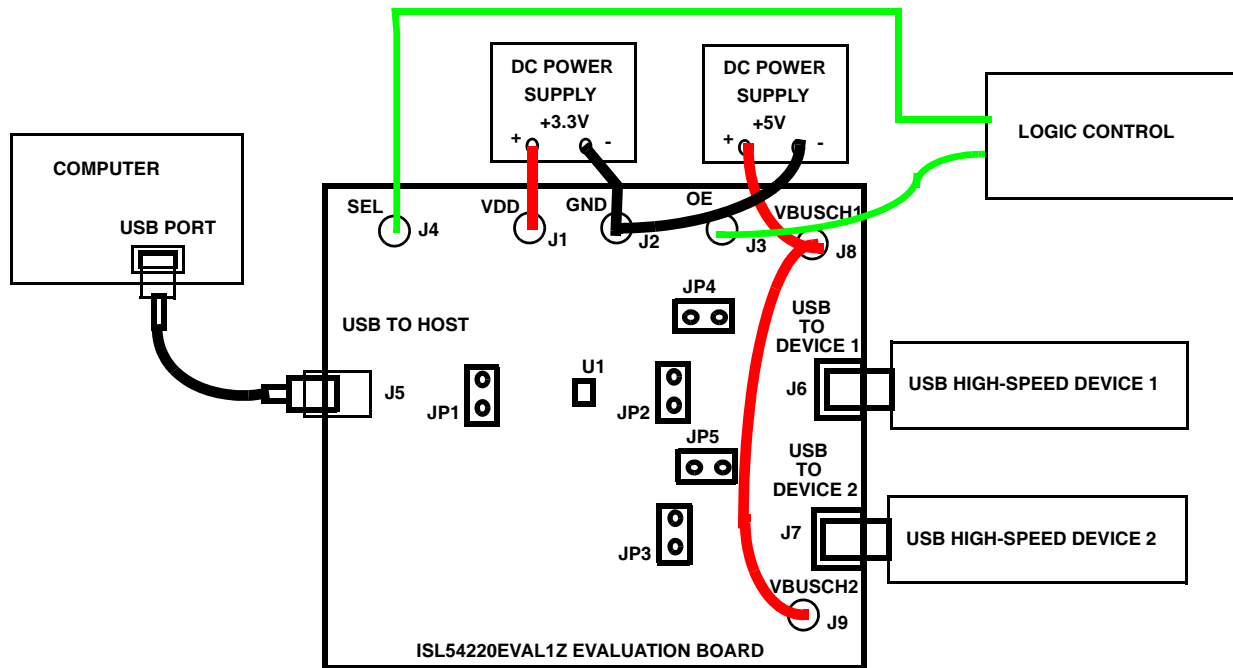
The maximum normal operating signal range for the HSx switches is from 0V to  $V_{DD}$ . The signal voltage should not be allowed to exceed the  $V_{DD}$  voltage rail or go below ground by more than -0.3V for normal operation.

However, in the event that the USB 5.25V  $V_{BUS}$  voltage gets shorted to one or both of the D-/D+ pins, the ISL54220 has

special fault protection circuitry to prevent damage to the ISL54220 part. The fault circuitry allows the signal pins (D-, D+, HS1D-, HS1D+, HS2D-, HS2D+) to be driven up to 5.5V while the  $V_{DD}$  supply voltage is in the range of 0V to 5.5V. In this condition the part draws  $< 500\mu A$  of current and causes no stress to the IC. In addition, when  $V_{DD}$  is at 0V (ground), all switches are OFF and the fault voltage is isolated from the other side of the switch. When  $V_{DD}$  is in the range of 2.7V to 5.5V, the fault voltage will pass through to the output of an active switch channel.

### Board Component Definitions

DESIGNATOR	DESCRIPTION
U1	ISL54220IRUZ IC
J5	"B" type USB Receptacle
J6, J7	"A" type USB Receptacle
J1	$V_{DD}$ Positive Connection
J2	$V_{DD}$ Negative Connection
J4	SEL Logic Control
J7	$\overline{OE}$ Logic Control
J8	$V_{BUS}$ Voltage for Highspeed Device 1
J9	$V_{BUS}$ Voltage for Highspeed Device 2
JP1, JP2, JP3	D-/D+ Differential Probe Connection
JP4, JP5	Host Controller $V_{BUS}$ Jumper



NOTE: DISCONNECT THE +5V POWER SUPPLY CONNECTED TO J8 AND J9 WHEN POWERING THROUGH HOST CONTROLLER BUS.

FIGURE 2. BASIC EVALUATION TEST SETUP BLOCK DIAGRAM

## Using The Board (Refer to Figure 2)

### Lab Equipment

The equipment, external supplies and signal sources needed to operate the board are listed in the following:

1. +3.3V to +5V DC Power Supply
2. +5V DC Power Supply
3. Two High-Speed USB device (i.e. USB memory stick, MP3 Player, etc.)
4. Computer with 2.0 High-Speed USB port
5. Standard USB cable
6. Logic Controller

### Initial Board Setup Procedure

1. Attach the main evaluation board to a DC power supply at J1 (VDD) and J2 (GND). Positive terminal at J1 and negative terminal at J2. The supply should be capable of delivering 2.7V to 5V and 100µA of current. Set the supply voltage to 3.3V.
2. Connect a DC power supply at J8 (VBUSCH1) and J9 (VBUSCH2). Positive terminal at J8 and J9 and negative terminal at J2 (GND). The supply should be capable of delivering 5V and 100mA of current. Set the supply voltage to 5V. This supply will provide 5V at the V<sub>BUS</sub> pin of the USB "A" type connectors, J6 and J7.
3. Connect a one high-speed USB device at USB connector J6 and the other high-speed USB device at USB connector J7. These connectors are located on the right side of the evaluation board.

4. Drive the  $\overline{OE}$  control pin HIGH to open all switches of the ISL54220 IC.
5. Connect USB cable from host (PC computer) to the USB "B" type receptacle, J5 (USB TO HOST).

### High-Speed Channel 1 Operation

1. Apply a logic LOW to the SEL pin.
2. Apply a logic LOW to the  $\overline{OE}$  pin.
3. You should now be able to send and receive data between the computer and the USB device 1 connected at J6.
4. To disconnect the USB device 1 from the computer, take the  $\overline{OE}$  pin HIGH.

### High-Speed Channel 2 Operation

1. Apply a logic HIGH to the SEL pin.
2. Apply a logic LOW to the  $\overline{OE}$  pin.
3. You should now be able to send and receive data between the computer and USB device 2 connected at J7.

### Test Points

The board has various test points for ease of connecting probes to make measurements. The test points available are described in Table 1.

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TABLE 1.

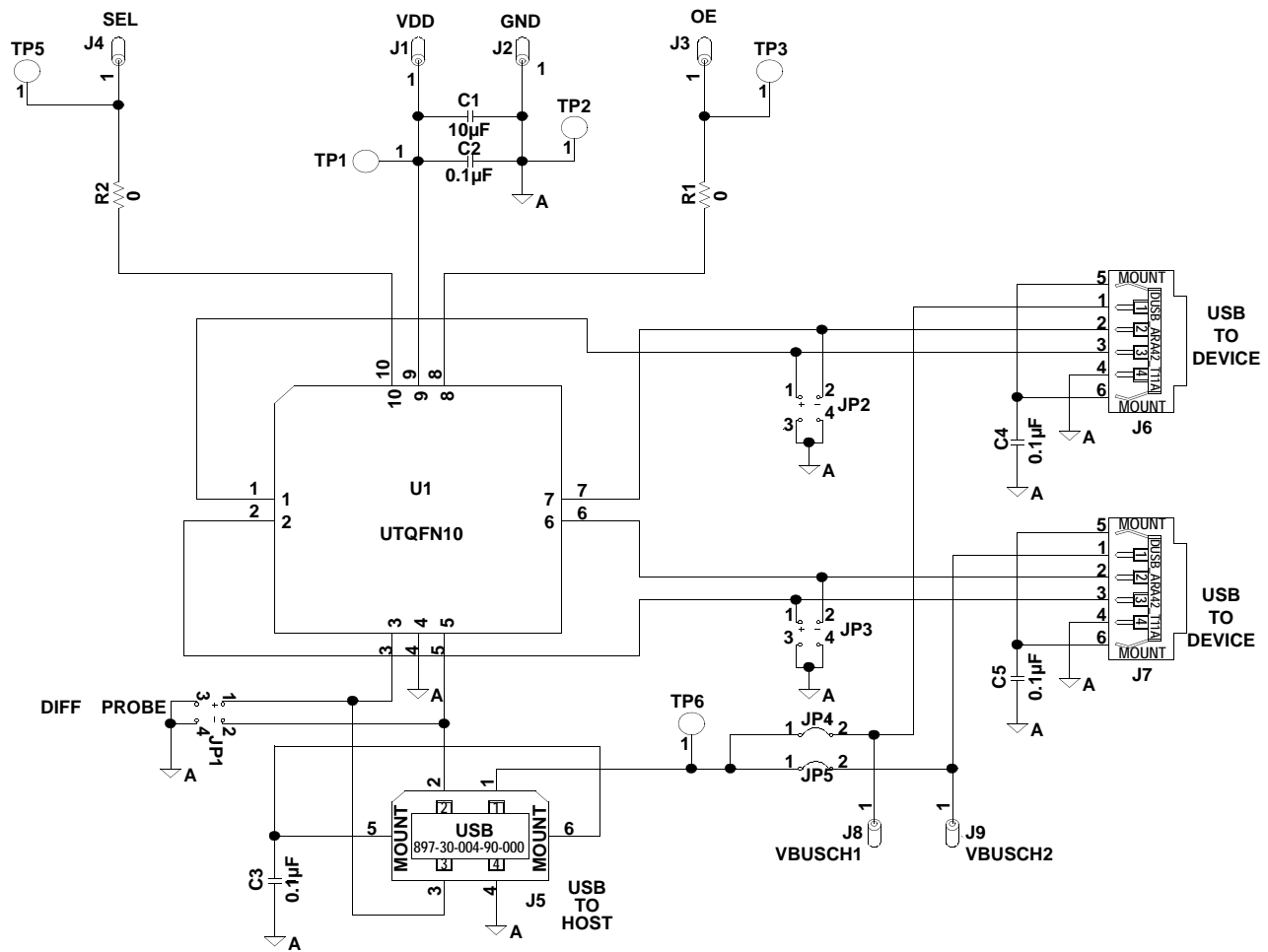
DESIGNATOR	DESCRIPTION
TP1	V <sub>DD</sub> test point
TP2	Ground Test Point
TP3	$\overline{OE}$ Test Point
TP5	SEL Test Point
TP6	V <sub>BUS</sub> from Pin 1 of Connector J5 Test Point
JP1	D-/D+ Differential Probe Connection - COM Side of Switch
JP2	D-/D+ Differential Probe Connection - Device 1-Side of Switch
JP3	D-/D+ Differential Probe Connection - Device 2-Side of Switch

You can observe the D- and D+ USB signal of the high-speed Channel 1 on an oscilloscope or other test equipment by connecting a differential probe at JP2.

You can observe the D- and D+ USB signal of the high-speed Channel 2 on an oscilloscope or other test equipment by connecting a differential probe at JP3.

You can observe the D- and D+ USB signal at the COM side of the switch on an oscilloscope or other test equipment by connecting a differential probe at JP1.

## ISL54220IRUEVAL1Z Board Schematic



Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that the Application Note or Technical Brief is current before proceeding.

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